REMARKS

Present Status of the Application

The Office Action claims 1-3, 7, 8, 10 and 11 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The Office Action claims 1-3, 7, 8, 10 and 11 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly pointed and distinctly claim the subject matter which applicant regards as the invention. The Office Action rejected claims 1, 7 and 8 under 35 U.S.C. 102(b), as being anticipated by Sparks (U.S. 6,062,461). The Office Action rejected claims 1, 3, 7, 8 and 11 under 35 U.S.C. 102(a), as being anticipated by Suda (U.S. 6,635,941). The Office Action also rejected claims 2 and 10 under 35 U.S.C. 103(a) as being unpatentable over Suda or Sparks (U.S. 6,062,461).

Applicant has amended the specification to correct the translation errors. Applicant has also amended claims 1-11, in which claims 4-6 and 9 are withdrawn, to more clearly define the present invention. After entry of the foregoing amendments, claims 1-3, 7, 8, 10 and 11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Rejection under 35 U.S.C 112, first paragraph

The office action points out that the limitation "solidifying the frame" in claims 1, 3, 7 was not described in the specification in such a way as to enable one skilled in the art to which it pertains or perform the step of solidifying the frame since it is uncertain as to whether the frame being liquid, gel, foam or resin, etc material and how the frame is formed on the chip.

Applicant has amended the term of "frame" into "frame sealant" in the whole specification and claims to correct the translation errors, and no new matter is entered because:

In the paragraph [0004] of the specification, the admitted prior art discloses a glass substrate is attached to the chip using a frame such that a sealed space is formed and prevents moistures and particles from the sealed space. Apparently, the term "frame" is "frame sealant" because a sealed space can be formed after attaching the glass substrate to the chip. In addition, US 6,063,646 also described that a sealant layer is used in a wafer package process. Using a sealant in a package process is well known to the people skilled in the art. In particular, because the sealant is usually formed around a chip in a package process, it has a shape of frame. Therefore, applicant respectfully submits the term of "frame" is an obvious error in translation and technical description. An amendment to correct an obvious translation error does not constitute new matter (In re Oda, 443 F.2d 1200, 170 USPQ 268 (C.C.P.A. 1971). Obvious errors in technical description that can be detected and corrected based on the application disclosure can be corrected (*Ex parte Brodbeck*, 199 USPQ 230 (Pat. Off. Bd. App. 1977)).

Because the term of "frame" is amended into "frame sealant", and the specification has described "the method of solidifying the sealant frame is accomplished by exposing the frame sealant 330 to an ultraviolet light or by using some other methods" in paragraph [0024], applicant respectively submits the step of "solidifying the frame sealant" in claims 1, 3, 7 has been complied with the enablement requirement.

Additionally, applicant also amended the title of the present invention "frame attaching process" into "package process" to more particularly direct to the subject matter which applicant regards as the present invention.

Rejection under 35 U.S.C 112, second paragraph

The office action points out the limitation "attaching the substrate to frame on chip under a negative pressure" in claims 1 and 7 is vague because it is unclear as to whether all the attaching elements are under a negative pressure or only the chip. Applicant has amended claims 1 and 7 in which the step of placing the transparent substrate and the chip in a vacuum system before the step of attaching the substrate to frame on chip under a negative pressure is added. Therefore, in the present invention, all the attaching elements are under a negative pressure.

The office action points out the limitation "solidifying the frame" is incomplete since it is uncertain as to what material the frame made of and how the frame is formed in prior to the solidifying step. Applicant has amended the term of "frame" into "frame sealant", and claims 3 and 11 and paragraph [0024] describe the step of solidifying the sealant frame is performed by exposing the frame sealant to an ultraviolet light, and therefore applicant respectively submits the limitation "solidifying the frame" is complete.

Rejection under 35 U.S.C 102

Applicants respectfully traverse the 102(b) rejection of claims 1, 7 and 8 because Sparks (U.S. 6,062,461) does not teach every element recited in these claims. Applicants also respectfully traverse the 102(a) rejection of claims 1, 3, 7, 8 and 11 because Suda (U.S. 6,635,941) does not teach every element recited in these claims.

> In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is in general related a package process as claims 1 and 7 recite:

Claim 1. A package process adapted to attach an attaching surface of a transparent substrate to an active area of a chip by a frame sealant, the active area of the chip comprising a functional area, the package process comprising:

forming the frame sealant on the active area of the chip, the frame sealant surrounding the functional area;

placing the transparent substrate and the chip in a vacuum system and attaching the attaching surface of the transparent substrate to the frame sealant formed on the active area of the chip under a negative pressure; and

solidifying the frame sealant.

Claim 7. A package process adapted to attach an attaching surface of a transparent substrate to an active area of a chip using a frame sealant, the active area of the chip comprising a functional area, the package process comprising:

placing the transparent substrate and the chip in a vacuum system;

attaching the attaching surface of the transparent substrate to the active area of the chip using the frame sealant under a negative pressure, the frame sealant surrounding the functional area; and

solidifying the frame sealant.

Sparks teaches a process for bonding micromachined wafers using solders, as Fig. 1 shown. The solderable rings 18, 20 are formed on the device wafer 10 and the capping wafer 12 respectively, and then a wafer bonding process is performed such that the solderable rings 18, 20 are bonded together. However, in claim 1 of the present application, a frame sealant is formed on the chip, and the transparent substrate and the chip are attached together through the frame sealant under a negative pressure. In claim 7 of the present invention, a transparent substrate and a chip is attached using a frame sealant under a negative pressure. Sparks fails to teach that

bonding a wafer and a substrate through a frame sealant, and the bonding step is performed under a negative pressure. Therefore, Sparks does not teach every element recited in claims 1 and 7.

In addition, Suda fails to disclose, teach or suggest the transparent substrate and the chip are placed in a vacuum system to perform the step of attaching the transparent substrate and the chip under a negative pressure. Suda discloses the wafer 910 is sucked when the optical element sets 907 are bonded in order to remove the warp of the wafer 910 (see col. 9, lines 29-33). In other words, only the wafer is under a negative pressure when the bonding step is carried out. However, in claims 1 and 7, the transparent substrate and the chip are placed into a vacuum system before performing the attaching step, and thus both the transparent substrate and the chip are under a negative pressure when the attaching step is performed. Therefore, Suda fails to teach every element in claims 1 and 7.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 7 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 3, 8 and 11 patently define over the prior art as a matter of law.

Rejection under 35 U.S.C 103 (a)

The Office Action rejected claims 2 and 10 under 35 U.S.C. 103(a), as being unpatentable over Suda or Sparks. Applicant respectfully traverses the rejections for at least the reasons set forth below.

Applicant submits that, as disclosed above, Suba and Sparks fail to teach or suggest each and every element of claims 1, 7, from which claims 2 and 10 depend. As discussed above

mentioned, independent claims 1 and 7 are patentable over Suba and Sparks. For at the least the same reasons, their dependent claims 2 and 10 are also patentable as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claim.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 3/21/2006

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809